STA308A

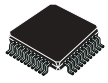
MULTICHANNEL DIGITAL AUDIO PROCESSOR WITH DDX™

PRODUCT PREVIEW

1 FEATURES

- 8 Channels of 24-bit DDX™
- >100dB SNR and Dynamic Range
- Selectable 32kHz-192kHz Input Sample Rates
- 6 Channels of DSD/SACD Input
- I^2C control with Selectable Device Address
- Digital Gain/Attenuation +58dB to -100dB in 0.5dB steps
- Soft Volume Update
- Individual Channel and Master Gain/ Attenuation plus Channel Trim (-10dB to +10dB)
- Up to 10 Independent 32-bit User Programmable Biquads (EQ) per channel
- Bass/Treble Tone Control
- Pre and Post EQ Full 8-Channel Input Mix on all 8 Channels
- Dual Independent Limiters/Compressors
- Dynamic Range Compression or Anti-Clipping Modes
- AutoModes™:
  - 5-Band Graphic EQ
  - 32 Preset EQ Curves (Rock, Jazz, Pop, etc.)
  - Automatic Volume Controlled Loudness
  - 5.1 to 2 channels Channels Downmix
  - Simultaneous 5.1 and 2 Channel Downmix Outputs
  - 3 Preset Volume Curves
  - 2 Preset Anti-Clipping Modes
  - Preset Movie Nighttime Listening Mode
  - Preset TV Channel/Commercial AGC Mode
  - 5.1 Bass Management Configurations
  - 2.1 Bass Management
  - AM Frequency Automatic Output PWM Frequency Shifting
  - QSurround5.1
  - 8 preset Crossover filters
- Individual Channel and Master Soft and Hard Mute
- Automatic Zero-Detect Mute
- Automatic Invalid Input Detect Mute
- Advanced PopFreeTM Operation
- Advanced AM Interference Frequency Switching and Noise Suppression Modes

Figure 1. Package



TQFP64

Table 1. Order Code

Part Number	Package
STA308A	TQFP64

- PSCorrectTM Power Supply Ripple Correction
- 8-Channel I2S Input and Output Data Interface
- I2S Output Channel Mapping Function
- Independent Channel Volume and DSP Bypass
- Channel Mapping of any input to any processing/DDX channel
- DC Blocking Selectable High-Pass Filter
- Selectable per-channel DDX Damped Ternary or Binary PWM output
- Selectable De-emphasis
- Variable Max Power Correction for lower full-power THD
- Variable per channel DDX output delay control
- PWM Half and Double Speed Modes
- Internal Loop Mode for up to 1 Channel of 80 Programmable Biquads
- 192kHz Internal Processing Sample Rate, 24-bit to 36-bit precision
- 3.3V Single Supply Operation

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2 DESCRIPTION

The STA308A is a single chip solution for digital audio processing and control in multi-channel applications. It provides output capabilities for DDX™ (Direct Digital Amplification). In conjunction with a DDX™ power device, it provides high-quality, high-efficiency, all digital amplification. The device is extremely versatile allowing for input of most digital formats including 6.1/7.1 channel and 192kHz, 24-bit DVD-Audio, DSD/SACD. In 5.1 application the additional 2

This is preliminary information on a new product now in development. Details are subject to change without notice.

DESCRIPTION (continued)

channels can be used for line-out or loadphone drive

Figure 2. BLOCK DIAGRAM

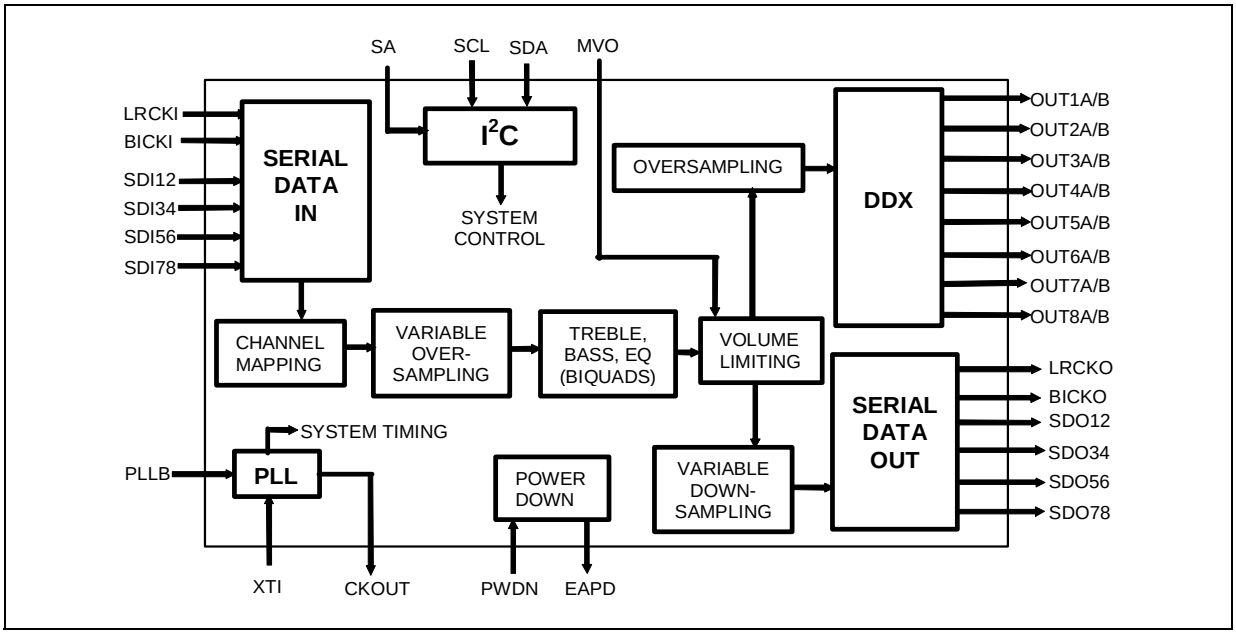


Figure 3. CHANNEL SIGNAL FLOW

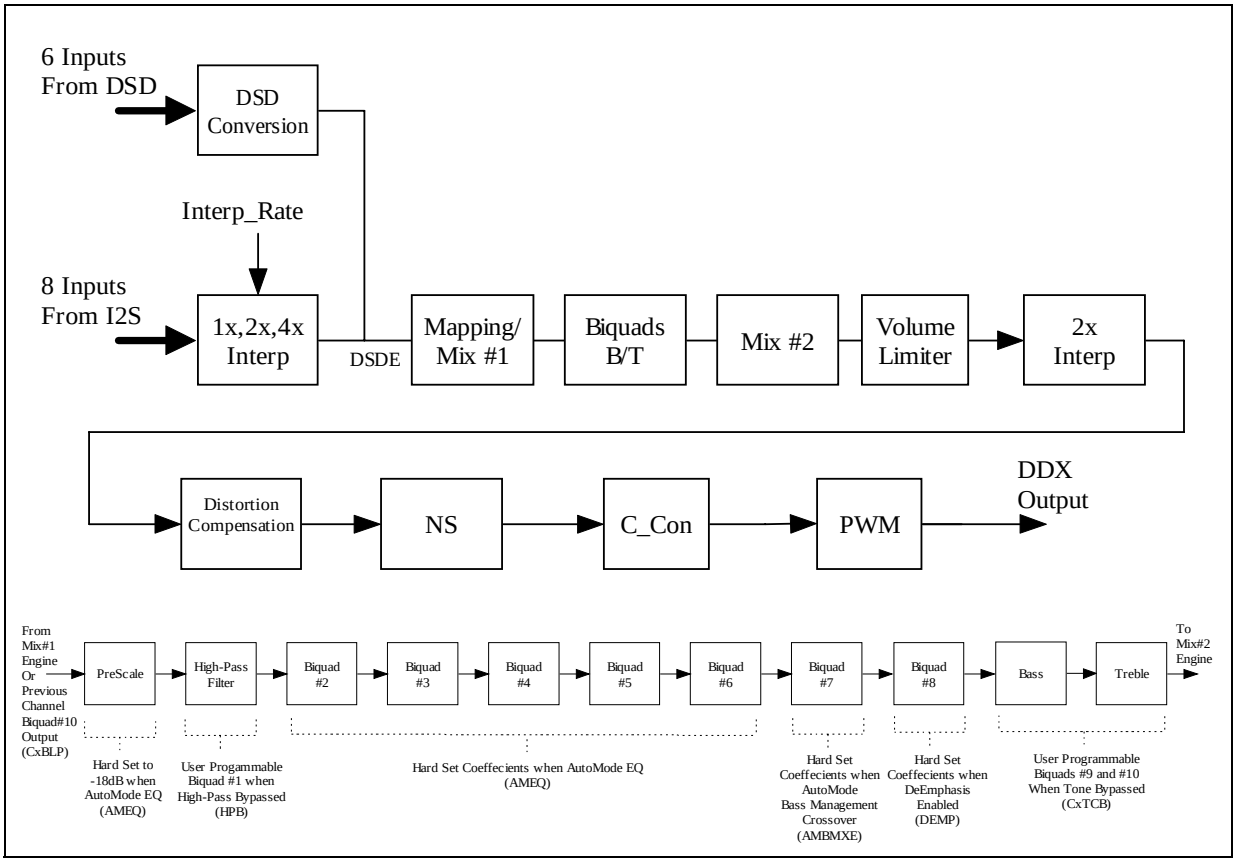


Figure 4. PIN CONNECTION (Top view)

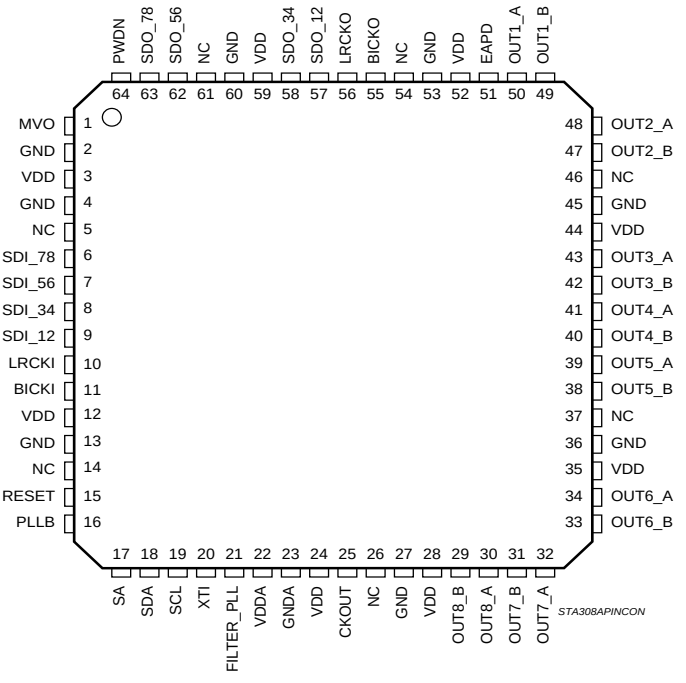


Table 2. PIN FUNCTION

PIN	NAME	DESCRIPTION	PAD TYPE
1	MVO/DSD_CLK	Master Volume Override/ DSD Input Clock	5V Tolerant TTL Input Buffer
6	SDI_78/DSD_6	Input Serial Data Channels 7 & 8/ DSD Input Channel 6	5V Tolerant TTL Input Buffer
7	SDI_56/DSD_5	Input Serial Data Channels 5 & 6/ DSD Input Channel 5	5V Tolerant TTL Input Buffer
8	SDI_34/DSD_4	Input Serial Data Channels 3 & 4/ DSD Input Channel 4	5V Tolerant TTL Input Buffer
9	SDI_12/DSD_3	Input Serial Data Channels 1 & 2/ DSD Input Channel 3	5V Tolerant TTL Input Buffer
10	LRCKI/DSD_2	Input Left/Right Clock/ DSD Input Channel 2	5V Tolerant TTL Input Buffer
11	BICKI/DSD_1	Input Serial Clock/ DSD Input Channel 1	5V Tolerant TTL Input Buffer
15	RESET	Global Reset	5V Tolerant TTL Schmitt Trigger Input Buffer
16	PLL_BYPASS	Bypass Phase Locked Loop	CMOS Input Buffer with Pull-Down
17	SA	Select Address (I^2C)	CMOS Input Buffer with Pull-Down
18	SDA	I^2C Serial Data	Bidirectional Buffer: 5V Tolerant TTL Schmitt Trigger Input; 3.3V Capable 2mA Slew-rate controlled Output.
19	SCL	I^2C Serial Clock	5V Tolerant TTL Schmitt Trigger Input Buffer
20	XTI	Crystal Oscillator Input (Clock Input)	5V Tolerant TTL Schmitt Trigger Input Buffer
21	FILTER_PLL	PLL Filter	Analog Pad
22	VDDA	PLL Supply	3.3V Analog Power Supply Voltage
23	GNDA	PLL Ground	Analog Ground
25	CKOUT	Clock Output	3.3V Capable TTL Tristate 4mA Output Buffer
29	OUT8B	PWM Channel 8 Output B	3.3V Capable TTL 2mA Output Buffer

Table 2. PIN FUNCTION (continued)

PIN	NAME	DESCRIPTION	PAD TYPE
30	OUT8A	PWM Channel 8 Output A	3.3V Capable TTL 2mA Output Buffer
31	OUT7B	PWM Channel 7 Output B	3.3V Capable TTL 2mA Output Buffer
32	OUT7A	PWM Channel 7 Output A	3.3V Capable TTL 2mA Output Buffer
33	OUT6B	PWM Channel 6 Output B	3.3V Capable TTL 2mA Output Buffer
34	OUT6A	PWM Channel 6 Output A	3.3V Capable TTL 2mA Output Buffer
38	OUT5B	PWM Channel 5 Output B	3.3V Capable TTL 2mA Output Buffer
39	OUT5A	PWM Channel 5 Output A	3.3V Capable TTL 2mA Output Buffer
40	OUT4B	PWM Channel 4 Output B	3.3V Capable TTL 2mA Output Buffer
41	OUT4A	PWM Channel 4 Output A	3.3V Capable TTL 2mA Output Buffer
42	OUT3B	PWM Channel 3 Output B	3.3V Capable TTL 2mA Output Buffer
43	OUT3A	PWM Channel 3 Output A	3.3V Capable TTL 2mA Output Buffer
47	OUT2B	PWM Channel 2 Output B	3.3V Capable TTL 2mA Output Buffer
48	OUT2A	PWM Channel 2 Output A	3.3V Capable TTL 2mA Output Buffer
49	OUT1B	PWM Channel 1 Output B	3.3V Capable TTL 2mA Output Buffer
50	OUT1A	PWM Channel 1 Output A	3.3V Capable TTL 2mA Output Buffer
51	EAPD	Ext. Amp Power Down	3.3V Capable TTL 4mA Output Buffer
55	BICKO	Output Serial Clock	3.3V Capable TTL 2mA Output Buffer
56	LRCKO	Output Left/Right Clock	3.3V Capable TTL 2mA Output Buffer
57	SDO_12	Output Serial Data Channels 1&2	3.3V Capable TTL 2mA Output Buffer
58	SDO_34	Output Serial Data Channels 3&4	3.3V Capable TTL 2mA Output Buffer
3,12,24,28,35,44,52,59	VDD	3.3V Supply	3.3V Digital Power Supply Voltage
2,4,13,27,36,45,53,60	GND	Ground	Digital Ground
5,14,26,37,46,54,61	NC	No Connect	
62	SDO_56	Output Serial Data Channels 5&6	3.3V Capable TTL 2mA Output Buffer
63	SDO_78	Output Serial Data Channels 7&8	3.3V Capable TTL 2mA Output Buffer
64	PWDN	Device Powerdown	5V Tolerant TTL Schmitt Trigger Input Buffer

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	3.3V I/O Power Supply	-0.5 to 4	V
V_{DDA}	3.3V Logic Power Supply	-0.5 to 4	V
V_i	Voltage on input pins	-0.5 to (VDD+0.5)	V
V_o	Voltage on output pins	-0.5 to (VDD+0.3)	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_{amb}	Ambient Operating Temperature	-20 to +85	°C

Table 4. THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance Junction to Ambient	85	°C/W

Table 5. RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	I/O Power Supply	3.0 to 3.6	V
V_{DDA}	Logic Power Supply	3.0 to 3.6	V
T_j	Operating Junction Temperature	-20 to +125	°C

3 ELECTRICAL CHARACTERISTCS (V_{DD3} = 3.3V ± 0.3V; V_{DDA} = 3.3V ± 0.3V; T_{AMB} = 0 TO 70 °C; UNLESS OTHERWISE SPECIFIED)

Table 6. GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{il}	Low Level Input no pull-up	V_i = 0V			1	µA	1
I_{ih}	High Level Input no pull-down	$V_i = V_{DD3}$			2	µA	1
I_{OZ}	Tristate output leakage without pullup/down	$V_i = V_{DD3}$			2	µA	1
V_{esd}	Electrostatic Protection	Leakage < 1µA	2000			V	2

Note 1: The leakage currents are generally very small, < 1na. The values given here are maximum after an electrostatic stress on the pin.
Note 2: Human Body Model

Table 7. DC ELECTRICAL CHARACTERISTICS: 3.3V BUFFERS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILhyst}	Low Level Threshold	Input Falling	0.8		1.35	V
V_{IHhyst}	High Level Threshold	Input Rising	1.3		2.0	V
V_{hyst}	Schmitt Trigger Hysteresis		0.3		0.8	V
V_{ol}	Low Level Output	Iol = 100uA			0.2	V
V_{oh}	High Level Output	Ioh = -100uA Ioh = -2mA	VDD3-0.2 2.4			V V

4 PIN DESCRIPTION

4.1 MVO: Master Volume Override

This pin enables the user to bypass the Volume Control on all channels. When MVO is pulled High, the Master Volume Register is set to 00h, which corresponds to its Full Scale setting. The Master Volume Register Setting offsets the individual Channel Volume Settings, which default to 0dB.

4.2 SDI_12 through 78: Serial Data In

Audio information enters the device here. Six format choices are available including I2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

4.3 RESET

Driving this pin (low) turns off the outputs and returns all settings to their defaults.

4.4 I^2C

The SA, SDA and SCL pins operate per the Philips I2C specification. See Section 5.

4.5 PLL: Phase Locked Loop

The phase locked loop section provides the System Timing Signals and CKOUT.

4.6 CKOUT: Clock Out

System synchronization and master clocks are provided by the CKOUT.

4.7 OUT1 through OUT8: PWM Outputs

The PWM outputs provide the input signal for the power devices.

4.8 EAPD: External Amplifier Power-Down

This signal can be used to control the power-down of DDX power devices.

4.9 SDO_12 through 78: Serial Data Out

Audio information exits the device here. Six different format choices are available including I2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

4.10 PWDN: Device Power-Down

This puts the STA308A into a low-power state via appropriate power-down sequence. Pulling PWDN low begins power-down sequence, and EAPD goes low ~30ms later.

5 I^2C BUS SPECIFICATION

The STA308A supports the I^2C protocol via the input ports SCL and SDA_IN (Master to Slave) and the output port SDA_OUT (Slave to Master).

This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver.

The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA308A is always a slave device in all of its communications.

5.1 COMMUNICATION PROTOCOL

5.1.1 Data Transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

5.1.2 Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 Stop Condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA308A and the bus master.

5.1.4 Data Input

During the data input the STA308A samples the SDA signal on the rising edge of clock SCL.

For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

5.2 DEVICE ADDRESSING

To start communication between the master and the Omega DDX core, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I^2C bus definition. In the STA308A the I^2C interface has two device addresses depending on the SA port configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8^{th} bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA308A identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9^{th} bit time. The byte following the device identification byte is the internal space address.

5.3 WRITE OPERATION

Following the START condition the master sends a device select code with the RW bit set to 0. The STA308A acknowledges this and the writes for the byte of internal address.

After receiving the internal byte address the STA308A again responds with an acknowledgement.

5.3.1 Byte Write

In the byte write mode the master sends one data byte, this is acknowledged by the Omega DDX Core. The master then terminates the transfer by generating a STOP condition.

5.3.2 Multi-byte Write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 5. Write Mode Sequence

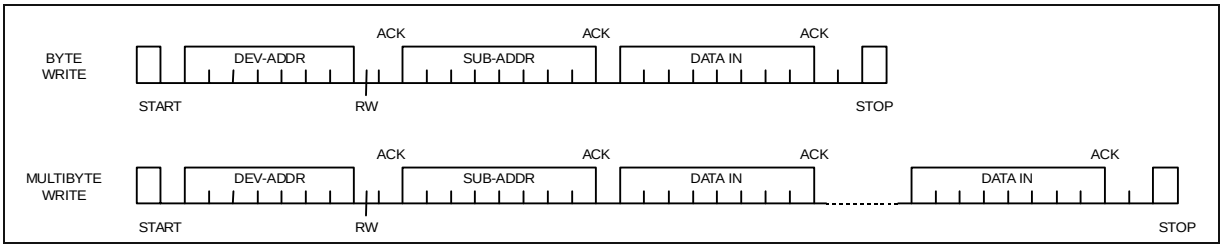
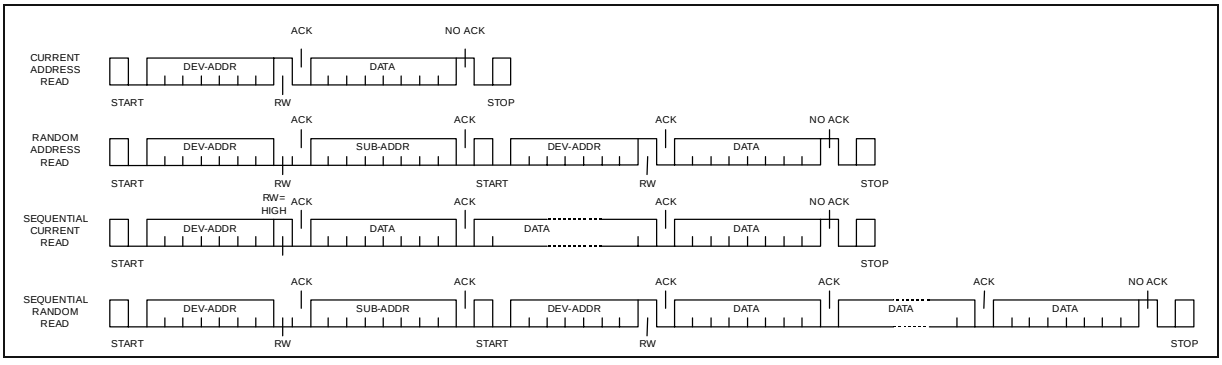


Figure 6. Read Mode Sequence



6 REGISTER SUMMARY

Table 8. Register Summary

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	ConfA	COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
0x01	ConfB				SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	ConfC				SAOFB	SAO3	SAO2	SAO1	SAO0
0x03	ConfD	MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x04	ConfE	C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0x05	ConfF	PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0x06	ConfG	MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0x07	ConfH	ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0x08	ConfI	EAPD							PSCE
0x09	Mmute								MMute
0x0A	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x0B	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x0C	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0D	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0E	C4Vol	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0x0F	C5Vol	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0x10	C6Vol	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0x11	C7Vol	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0x12	C8Vol	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0x13	C1VTMB	C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0x14	C2VTMB	C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0x15	C3VTMB	C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0x16	C4VTMB	C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0x17	C5VTMB	C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0x18	C6VTMB	C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0x19	C7VTMB	C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0x1A	C8VTMB	C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
0x1B	C12im		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
0x1C	C34im		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
0x1D	C56im		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
0x1E	C78im		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
0x1F	Auto1	AMDM	AMGC2	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0x20	Auto2	SUB	RSS1	RSS0	CSS1	CSS0	FSS	AMBMXE	AMBMME
0x21	Auto3	AMAM2	AMAM1	AMAM0	AMAME			MSA	AMPS
0x22	PreEQ	XO2	XO1	XO0	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
0x23	Ageq				AGEQ4	AGEQ3	AGEQ2	AGEQ1	AGEQ0
0x24	Bgeq				BGEQ4	BGEQ3	BGEQ2	BGEQ1	BGEQ0
0x25	Cgeq				CGEQ4	CGEQ3	CGEQ2	CGEQ1	CGEQ0
0x26	Dgeq				DGEQ4	DGEQ3	DGEQ2	DGEQ1	DGEQ0
0x27	Fgeq				EGEQ4	EGEQ3	EGEQ2	EGEQ1	EGEQ0
0x28	BQlp	C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP

Table 8. Register Summary (continued)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x29	MXlp	C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
0x2A	EQbp	C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQBP	C3EQBP	C2EQBP	C1EQBP
0x2B	ToneBP	C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
0x2C	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x2D	C1234ls	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0x2E	C5678ls	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0x2F	L1ar	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x30	L1atrt	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x31	L2ar	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x32	L2atrt	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x33	C12ot		C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
0x34	C34ot		C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
0x35	C56ot		C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
0x36	C78ot		C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
0x37	C12om		C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
0x38	C34om		C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
0x39	C56om		C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
0x3A	C78om		C8OM2	C8OM1	C8OM0		C7OM2	C7OM1	C7OM0
0x3B	Cfaddr1							CFA9	CFA8
0x3C	Cfaddr2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x3D	B1cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x3E	B1cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x3F	B1cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x40	B2cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x41	B2cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x42	B2cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x43	A1cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x44	A1cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x45	A1cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x46	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x47	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x48	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x49	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x4A	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x4B	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x4C	Cfud							WA	W1
0x4D	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x4E	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x4F	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x50	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x51	PSC1	RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0x52	PSC2	RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0x53	PSC3	CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0

Table 8. Register Summary (continued)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x54	Qsnd						Qsfs	Qfour	Qen
0x55	Qsec1	Qsec15	Qsec14	Qsec13	Qsec12	Qsec11	Qsec10	Qsec9	Qsec8
0x56	Qsec2	Qsec7	Qsec6	Qsec5	Qsec4	Qsec3	Qsec2	Qsec1	Qsec0
0x57	BIST1		R6BACT	R5BACT	R4BACT	R3BACT	R2BACT	R1BACT	R0BACT
0x58	BIST2		R6BEND	R5BEND	R4BEND	R3BEND	R2BEND	R1BEND	R0BEND
0x59	BIST3		R6BBAD	R5BBAD	R4BBAD	R3BBAD	R2BBAD	R1BBAD	R0BBAD

6.1 Configuration Register A (address 00h)

D7	D6	D5	D4	D3	D2	D1	D0
COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
1	0	0	0	0	0	1	1

6.1.1 Master Clock Select

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	1	MCS0	Master Clock Select : Selects the ratio between the input I^2S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The DDX8000 will support sample rates of 32kHz, 44.1kHz, 48Khz, 88.2kHz, 96kHz, 176.4kHz, 192kHz, and 2.8224MHz DSD. Therefore the internal clock will be:

- 65.536Mhz for 32kHz
- 90.3168Mhz for 44.1khz, 88.2kHz, 176.4kHz, and DSD
- 98.304Mhz for 48kHz, 96kHz, and 192kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency(fs). The relationship between the input clock and the input sample rate is determined by both the MCSx and the IRx (Input Rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IRx bits determine the oversampling ratio used internally.

Table 9.

Input Sample Rate *fs* (kHz)	IR	MCS(2..0)				
		1xx	011	010	001	000
32, 44.1, 48	00	128fs	256fs	384fs	512fs	768fs
88.2, 96	01	64fs	128fs	192fs	256fs	384fs
176.4, 192	10	64fs	128fs	192fs	256fs	384fs
DSD	11	2fs	4fs	6fs	8fs	10fs

6.1.2 Interpolation Ratio Select

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	IR0	Interpolation Ratio Select: Selects internal interpolation ratio based on input I^2S sample frequency
4	R/W	0	IR1	

The STA308A has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 4 times, 2 times, or 1 time (pass-through).

The oversampling ratio of this interpolation is determined by the IR bits.

Table 10. IR bit settings as a function of Input Sample Rate.I

Input Sample Rate *Fs* (kHz)	IR(1,0)	1st Stage Interpolation Ratio
32	00	4 times oversampling
44.1	00	4 times oversampling
48	00	4 times oversampling
88.2	01	2 times oversampling
96	01	2 times oversampling
176.4	10	Pass-Through
192	10	Pass-Through
DSD	11	DSD -> 176.4kHz Conversion

6.1.3 DSP Bypass9

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	DSPB	DSP Bypass Bit: 0 – Normal Operation 1 – Bypass of Biquad and Bass/Treble Functionality

Setting the DSPB bit bypasses the biquad functionality of the Omega DDX Core.

6.1.4 Clock Output Select:

COS(1,0)	CKOUT Frequency
00	PLL Output
01	PLL Output/4
10	PLL Output/8
11	PLL Output/16

6.2 Serial Input Formats(Address 01h)

D7	D6	D5	D4	D3	D2	D1	D0
			SAIFB	SAI3	SAI2	SAI1	SAI0
			0	0	0	0	0

6.2.1

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	SAI0	Serial Audio Input Interface Format: Determines the interface format of the input serial digital audio interface.
1	R/W	0	SAI1	
2	R/W	0	SAI2	
3	R/W	0	SAI3	

6.2.2 Serial Data Interface

The STA308A audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. STA308A always acts a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI (pin xx), serial clock BICKI (pin xx), serial data 1 & 2 SDI12 (pin xx), serial data 3 & 4 SDI34 (pin xx), serial data 5 & 6 SDI56 (pin xx), and serial data 7 & 8 SDI78 (pin xx). The SAI register (Configuration Register x - xxh, Bits Dx-Dx) and the SAIFB register (Configuration Register x - 0xh, Bit Dx) are used to specify the serial data format. The default serial data format is I2S, MSB-First. Available formats are shown in the tables and figure that follow.

Table 11. Serial Data First Bit

SAIFB	Format
0	MSB-First
1	LSB-First

Note: Serial input and output formats (see section 8.2) are specified distinctly

For example, SAI=1110 and SAIFB=1 would specify Right-Justified 16-bit data, LSB-First.

Table 4 below lists the serial audio input formats supported by STA308A as related to BICKI = 32/48/64fs, where sampling rate fs = 32/44.1/48/88.2/96/176.4/192 kHz.

Table 12. Supported Serial Audio Input Formats

BICKI	SAI (3...0)	SAIFB	Interface Format
32fs	1100	X	I^2S 15bit Data
	1110	X	Left/Right-Justified 16bit Data
48fs	0100	X	I^2S 23bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0100	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data
64fs	0000	X	I^2S 24bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0000	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data

6.3

D7	D6	D5	D4	D3	D2	D1	D0
MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
1	1	0	0	0	0	1	0

6.3.1 DDX Power Output Mode

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	OM0	DDX Power Output Mode: Selects configuration of DDX output.
1	R/W	1	OM1	

The DDX Power Output Mode selects how the DDX output timing is configured. Different power devices use different output modes. The DDX-2060 recommended use is OM = 10.

Table 13. Output Modes

OM(1,0)	Output Stage – Mode
00	DDX-2060/2100 – Drop Compensation
01	Discrete Output Stage – Tapered Compensation
10	DDX-2060/2100 – Full Power Mode
11	Variable Drop Compensation (CSZx bits)

6.3.2 DDX Compensating Pulse Size Register

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	CSZ0	Contra Size Register: When OM(1,0) = 11, this register determines the size of the DDX compensating pulse from 0 clock ticks to 31 clock periods.
3	R/W	0	CSZ1	
4	R/W	0	CSZ2	
5	R/W	0	CSZ3	
6	R/W	1	CSZ4	

Table 14. Compensating Pulse Size

CSZ(4..0)	Compensating Pulse Size
00000	0 Clock period Compensating Pulse Size
00001	1 Clock period Compensating Pulse Size
…	…
11111	31 Clock period Compensating Pulse Size

6.3.3 Max Power Correction

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	MPC	Max Power Correction: Setting of 1 enables DDX-2060 correction for THD reduction near maximum power output.

Setting the MPC bit turns on special processing that corrects the DDX-2060 power device at high power. This mode should lower the THD+N of a full DDX-2060 DDX system at maximum power output and slightly below. This mode will only be operational in OM(1,0) = 01.

6.4

D7	D6	D5	D4	D3	D2	D1	D0
C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0	0	0	0	0	0	0	0

6.4.1 Binary Output Enable Registers

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	C1BO	Channels 1, 2, 3, 4, 5, 6, 7, & 8 Binary Output Mode Enable Bits. A setting of 0 indicates ordinary DDX tri-state output. A setting of 1 indicates binary output mode.
1	R/W	0	C2BO	
2	R/W	0	C3BO	
3	R/W	0	C4BO	
4	R/W	0	C5BO	
5	R/W	0	C6BO	
6	R/W	0	C7BO	
7	R/W	0	C8BO	

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel will be considered the positive output and output B is negative inverse.

6.5

D7	D6	D5	D4	D3	D2	D1	D0
PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0	0	0	0	0	0	0	0

6.5.1 High-Pass Filter Bypass

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	HPB	High-Pass Filter Bypass Bit. Setting of one bypasses internal AC coupling digital high-pass filter

The STA308A features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a DDX amplifier. DC signals can cause speaker damage.

If HPB = 1, then the filter that the high-pass filter utilizes is made available as user-programmable biquad#1.

6.5.2 Dynamic Range Compression/Anti-Clipping Bit

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	DRC	Dynamic Range Compression/Anti-Clipping 0 – Limiters act in Anti-Clipping Mode 1 – Limiters act in Dynamic Range Compression Mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the limiter settings.

In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a night-time listening mode that provides a reduction in the dynamic range regardless of the volume level.

6.5.3 De-Emphasis

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	DEMP	De-emphasis: 0 – No De-emphasis 1 – De-emphasis

By setting this bit to one de-emphasis will implemented on all channels. When this is used it takes the place of biquad #7 in each channel and any coefficients using biquad #1 will be ignored. DSPB(DSP Bypass) bit must be set to 0 for De-emphasis to function.

6.5.4 Post-Scale Link

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	PSL	Post-Scale Link: 0 – Each Channel uses individual Post-Scale value 1 – Each Channel uses Channel 1 Post-Scale value

Post-Scale functionality can be used for power-supply error correction. For multi-channel applications running off the same power-supply, the post-scale values can be linked to the value of channel 1 for ease of use and update the values faster.

6.5.5 Biquad Coefficient Link

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	BQL	Biquad Link: 0 – Each Channel uses coefficient values 1 – Each Channel uses Channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the Channel 1 Coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

6.5.6 PWM Speed Mode

BIT	R/W	RST	NAME	DESCRIPTION
7..5	R/W	00	PWMS(2..0)	PWM Speed Selection:

Table 15.

PWMS(1..0)	PWM Output Speed
000	Normal Speed(384kHz) All Channels
001	Half Speed(192kHz) All Channels
010	Double Speed(768kHz) All Channels
011	Normal Speed Channels 1-6, Double Speed Channels 7-8
100	Odd Speed(341.3kHz) All Channels

6.6

Table 16.

D7	D6	D5	D4	D3	D2	D1	D0
MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0	0	0	0	0	0	0	0

6.6.1 Output Signal Disables

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	PWMD	PWM Output Disable: 0 - PWM Output Normal 1 - No PWM Output
1	R/W	0	SID	Serial Interface(I^2S Out) Disable: 0 - I^2S Output Normal 1 - No I^2S Output
2	R/W	0	COD	Clock Output Disable: 0 - Clock Output Normal 1 - No Clock Output

6.6.2 AM Mode Enable

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	AME	AM Mode Enable: 0 – Normal DDX operation. 1 – AM reduction mode DDX operation.

The STA308A features a DDX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when DDX is operating in a device with an AM tuner active. The SNR of the DDX processing is reduced to ~83dB in this mode, which is still greater than the SNR of AM radio.

6.6.3 AM2 Mode Enable

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	AM2E	AM2 Mode Enable: 0 – Normal DDX operation. 1 – AM2 reduction mode DDX operation.

The STA308A features a 2 DDX processing modes that minimize the amount of noise generated in frequency range of AM radio. This second mode is intended for use when DDX is operating in a device with an AM tuner active. This mode eliminates the noise-shaper.

6.6.4 Headphone Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	HPE	DDX Headphone Enable: 0 – Channels 7 & 8 normal DDX operation 1 – Channels 7 & 8 headphone operation

Channels 7 and 8 can be configured to be processed and output in such a manner that headphones can be driven using and appropriate output device. This signal is a fully differential 3-wire drive called DDX Headphone.

6.6.5 Distortion Compensation Variable Enable

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	0	DCCV	Distortion Compensation Variable Enable: 0 – Uses Preset DC Coefficient. 1 – Uses DCC Coefficient.

6.6.6 Max Power Correction Variable

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	MPCV	Max Power Correction Variable: 0 – Use Standard MPC Coefficient 1 – Use MPCC bits for MPC Coefficient

6.7 Conf H

Table 17.

D7	D6	D5	D4	D3	D2	D1	D0
ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0	1	1	1	1	1	1	0

6.7.1 Noise-Shaper Bandwidth Selection

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	NSBW	Noise-Shaper Bandwidth Selection: 1 – 3rd order NS 0 – 4th order NS

6.7.2 Zero-Crossing Volume Enable

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	1	ZCE	Zero-Crossing Volume Enable: 1 – Volume adjustments will only occur at digital zero-crossings 0 – Volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks will be audible.

6.7.3 Soft Volume Update Enable

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	1	SVE	Soft Volume Enable: 1 – Volume adjustments ramp according to SVR settings 0 – Volume adjustments will occur immediately

6.7.4 Zero-Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	1	ZDE	Zero-Detect Mute Enable: Setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the input data to each processing channel after the channel-mapping block. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled.

6.7.5 Invalid Input Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	1	IDE	Invalid Input Detect Mute Enable: Setting of 1 enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I2S data and will automatically mute if the signals are perceived as invalid.

6.7.6

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	1	BCLE	Binary Output Mode Clock Loss Detection Enable

Detects loss of input MCLK in binary mode and will output 50% duty cycle.

6.7.7

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	LDTE	LRCLK Double Trigger Protection Enable

Actively prevents double trigger of LRCLK.

6.7.8

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	ECLE	Auto EAPD on Clock Loss

When active will issue a power device power down signal(EAPD) on clock loss detection

6.8 Conf

Table 18. I

D7	D6	D5	D4	D3	D2	D1	D0
EAPD							PSCE
0							0

6.8.1 PSCorrect™ Enable

This feature utilizes an ADC on SDI78 that provides power supply ripple information for correction. Registers PSC1, PSC2, PSC3 are utilized in this mode.

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	PSCE	Power Supply Ripple Correction Enable: 0 – Normal Operation 1 – PSCorrect Operation

6.8.2 External Amplifier Power Down

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	EAPD	External Amplifier Power Down: 0 – External Power Stage Power Down Active 1 – Normal Operation

6.8.3 Master Mute Register

D7	D6	D5	D4	D3	D2	D1	D0
							MMUTE
							0

6.8.4 Master Volume Register

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

Note : Value of volume derived from MVOL is dependent on AMV AutoMode Volume settings.

6.8.5 Channels 1,2,3,4,5,6,7,8 Mute

D7	D6	D5	D4	D3	D2	D1	D0
C8M	C7M	C6M	C5M	C4M	C3M	C2M	C1M
0	0	0	0	0	0	0	0

6.8.6 Channel 1 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

6.8.7 Channel 2 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

6.8.8 Channel 3 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

6.8.9 Channel 4 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0	1	1	0	0	0	0	0

6.8.10 Channel 5 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0	1	1	0	0	0	0	0

6.8.11 Channel 6 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0	1	1	0	0	0	0	0

6.8.12 Channel 7 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0	1	1	0	0	0	0	0

6.8.13 Channel 8 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0	1	1	0	0	0	0	0

6.8.14 Channel 1 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0	0	0	1	0	0	0	0

6.8.15 Channel 2 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0	0	0	1	0	0	0	0

6.8.16 Channel 3 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0	0	0	1	0	0	0	0

6.8.17 Channel 4 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0	0	0	1	0	0	0	0

6.8.18 Channel 5 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0	0	0	1	0	0	0	0

6.8.19 Channel 6 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0	0	0	1	0	0	0	0

6.8.20 Channel 7 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0	0	0	1	0	0	0	0

6.8.21 Channel 8 Volume Trim, Mute, Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
0	0	0	1	0	0	0	0

The Volume structure of the STA308A consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. There is also an additional offset for each channel called the channel volume trim. The individual channel volumes are adjustable in 0.5dB steps from +48dB to -78 dB. As an example if C5V = XXh or +XXXdB and MV = XXh or -XXdB, then the total gain for channel 5 = XXdB. The Channel Volume Trim is adjustable independently on each channel from -10dB to +10dB in 1 dB steps. The Master Mute when set to 1 will mute all channels at once, whereas the individual channel mutes(CxM) will mute only that channel. Both the Master Mute and the Channel Mutes provide a "soft mute" with the volume ramping down to mute in 8192 samples from the maximum volume setting at the internal processing rate(~192kHz). A "hard mute" can be obtained by commanding a value of all 1's(255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel that whose total volume is less than -91dB will be muted. All changes in volume take place at zero-crossings when ZCE = 1(configuration register B) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE=0, volume updates will occur immediately. Each channel also contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel. Each channel also contains a channel mute. If CxM = 1 a soft mute is performed on that channel.

Table 19. Master Volume Offset as a function of MV(7..0).

MV(7..0)	Volume Offset from Channel Value
00000000(00h)	0dB
00000001(01h)	-0.5dB
00000010(02h)	-1dB
…	…
01001100(4Ch)	-38dB
…	…
11111110(FEh)	-127dB
11111111(FFh)	Hard Master Mute

Table 20. Channel Volume as a function of CxV(7..0)

CxV(7..0)	Volume
00000000(00h)	+48dB
00000001(01h)	+47.5dB
00000010(02h)	+47dB
…	…
01100001(5Fh)	+0.5dB
01100000(60h)	0dB
01011111(61h)	-0.5dB
…	…
11111110(FEh)	-79.5 dB
11111111(FFh)	Hard Channel Mute

Table 21.

CxVT(4..0)	Volume
00000(00h)	+10dB
…	…
00110(06h)	+10dB
00111(07h)	+9dB
…	…
01111(0Fh)	+1dB
10000(10h)	0dB
10001(11h)	-1dB
…	…
11001(19h)	-9dB
11010(1Ah)	-10dB
…	…
11111(1Fh)	-10dB

6.9 Input Mapping

6.9.1 Channel Input Mapping Channels 1 & 2

D7	D6	D5	D4	D3	D2	D1	D0
	C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
	0	0	1		0	0	0

6.9.2 Channel Input Mapping Channels 3 & 4

D7	D6	D5	D4	D3	D2	D1	D0
	C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
	0	1	1		0	1	0

6.9.3 Channel Input Mapping Channels 5 & 6

D7	D6	D5	D4	D3	D2	D1	D0
	C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
	1	0	1		1	0	0

6.9.4 Channel Input Mapping Channels 7 & 8

D7	D6	D5	D4	D3	D2	D1	D0
	C8IM2	C8M1	C8IM0		C7IM2	C7IM1	C7IM0
	1	1	1		1	1	0

Each channel received via I2S can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing, simplifies output stage designs, and enables the ability to perform crossovers. The default settings of these registers map each I2S input channel to its corresponding processing channel.

Table 22. Channel mapping as a function of CxIM bits.

CxIM(2..0)	Serial Input From
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

6.10 AutoMode™ Registers:

6.10.1 Register - AutoModes EQ, Volume, GC

D7	D6	D5	D4	D3	D2	D1	D0
AMDM	AMGC2	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0	0	0	0	0	0	0	0

6.10.2 AutoMode EQ

AMEQ(1,0)	Mode(Biquad 2-6)
00	User Programmable
01	Preset EQ – PEQ bits
10	Graphic EQ – xGEQ bits
11	Auto Volume Controlled Loudness Curve

By setting AMEQ to any setting other than 00 enables AutoMode EQ, biquads 1-5 are not user programmable. Any coefficient settings for these biquads will be ignored. Also when AutoMode EQ is used the pre-scale value for channels 1-6 becomes hard-set to -18dB.

6.10.3 AutoMode Volume

AMV(1,0)	Mode(MVOL)
00	MVOL 0.5dB 256 Steps(Standard)
01	MVOL Auto Curve 30 Steps
10	MVOL Auto Curve 40 Steps
11	MVOL Auto Curve 50 Steps

6.10.4 AutoMode Gain Compression/Limiters

AMGC(2..0)	Mode
000	User Programmable GC
001	AC No Clipping
010	AC Limited Clipping(10%)
011	DRC Nighttime Listening Mode
100	DRC TV Commercial/Channel AGC
101	AC 5.1 No Clipping
110	AC 5.1 Limited Clipping(10%)

6.10.5 AMDM - Automode 5.1 Downmix

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	AMDM	0 – Normal Operation 1 – Channels 7-8 are 2 channel downmix of channels 1-6

Automode downmix setting uses channels 7-8 of Mix#1 engine and therefore these channels of this function are hard-set and not allowed to be user set when in this mode.

Channels 1-6 must be arranged via Channel Mapping (CxIM) if necessary in the following manner for this operation:

Channel 1 - Left
Channel 2 - Right
Channel 3 - Left Surround
Channel 4 - Right Surround
Channel 5 - Center
Channel 6 - LFE

6.10.6 Register - AutoModes Bass Management2

D7	D6	D5	D4	D3	D2	D1	D0
SUB	RSS1	RSS0	CSS1	CSS0	FSS	AMBMXE	AMBMME
1	0	0	0	0	0	0	0

6.10.7

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	AMBMME	0 – Automode Bass Management Mix Disabled 1 – Automode Bass Management Mix Enabled

6.10.8

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	AMBMXE	0 – Automode Bass Management Crossover Disabled 1 – Automode Bass Management Crossover Enabled

Setting the AMBMME bit enables the proper mixing to take place for various preset bass management configurations. Setting the AMBMXE bit enables the proper crossover filtering in biquad #7 to take place. The crossover for bass management is always 2nd order (24dB/octave) and the frequency of crossover is determined by the XOx bits in Preset EQ register.

All configurations of Dolby Bass-Management can be performed in the IC. These different configurations are selected as they would be by the end-user.

The AutoMode Bass Management Settings utilize Channels 1-6 on the Mix #1 engine, Channels 1-6 biquad #6, and Channels 1-2 on the Mix#2 engine in configuration #2. These functions cannot be user programmed while the bass management automode is active.

Not all settings are valid as some configurations are unlikely and do not have to be supported be Dolby Specification.

Automatic crossover settings are provided or custom crossovers can be implemented using the xxxxx settings in the RAM array.

Input Channels must be mapped using channel-mapping feature in the following manner for Bass Management to be performed properly.

1 - Left front

2 - Right front

3 - Left Rear

4 - Right Rear

5 - Center

6 - LFE

Table 23.

Register/Setting	10	01	00
CSS – Center Speaker Size	Off	Large	Small
RSS – Rear Speaker Size	Off	Large	Small

Table 24.

Register/Setting	1	0
FSS – Front Speaker Size	Large	Small
SUB - Subwoofer	On	Off

When AMBMXE = 1, biquad #7 on channels 1-6 are utilized for bass-management crossover filter, this biquad is not user programmable in this mode. The XO settings determine the crossover frequency used, the crossover is 2nd order for both high-pass and low-pass with a -3dB cross point. Higher order filters can be obtained be programming coefficients in other biquads if desired.

It is recommended to use settings of 120-160Hz when using small, single driver satellite speakers as the frequency response of these speakers normally are limited to this region.

6.10.9 Register - Auto3 AutoMode AM/Pre-Scale/Bass Management Scale

D7	D6	D5	D4	D3	D2	D1	D0
AMAM2	AMAM1	AMAM0	AMAME			MSA	AMPS
0	0	0	0			0	0

6.10.10

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	AMPS	AutoMode Pre-Scale 0 – -18dB used for Pre-scale when AMEQ /= 00 1 – User Defined Pre-scale when AMEQ /= 00

6.10.11

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	MSA	Bass Management Mix Scale Adjustment 0 – -12dB Scaling on satellite channels in Config #1 1 – No Scaling on satellite channels in Config #1

6.10.12

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	AMAME	AutoMode AM Enable 0 – Switching Frequency Determined by PWMS Settings 1 – Switching Frequency Determined by AMAM Settings

Table 25. AutoMode AM Switching Frequency Selection

AMAM(2..0)	48kHz/96kHz Input Fs	44.1kHz/88.2kHz Input Fs	
000	0.535MHz – 0.720MHz	0.535MHz – 0.670Mhz	N
001	0.721MHz – 0.900MHz	0.671MHz – 0.800MHz	O
010	0.901MHz – 1.100MHz	0.801MHz – 1.000MHz	N
011	1.101MHz – 1.300MHz	1.001MHz – 1.180MHz	O
100	1.301MHz – 1.480MHz	1.181MHz – 1.340Mhz	N
101	1.481MHz – 1.600MHz	1.341MHz – 1.500MHz	O
110	1.601MHz – 1.700MHz	1.501MHz – 1.700MHz	N

6.10.13 Register - Preset EQ Settings

D7	D6	D5	D4	D3	D2	D1	D0
XO2	XO1	XO0	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
1	0	1	0	0	0	0	0

Table 26.

XO(2..0)	Bass Management Crossover Frequency
000	70 Hz
001	80 Hz
010	90 Hz
011	100 Hz
100	110 Hz
101	120 Hz
110	140 Hz
111	160 Hz

Table 27.

PEQ(3..0)	Setting
00000	Flat
00001	Rock
00010	Soft Rock
00011	Jazz
00100	Classical
00101	Dance
00110	Pop
00111	Soft
01000	Hard
01001	Party
01010	Vocal
01011	Hip-Hop
01100	Dialog
01101	Bass-Boost #1
01110	Bass-Boost #2
01111	Bass-Boost #3
10000	Loudness 1
10001	Loudness 2
10010	Loudness 3
10011	Loudness 4
10100	Loudness 5
10101	Loudness 6
10110	Loudness 7
10111	Loudness 8
11000	Loudness 9
11001	Loudness 10
11010	Loudness 11
11011	Loudness 12
11100	Loudness 13
11101	Loudness 14
11110	Loudness 15
11111	Loudness 16

6.10.14Register – Graphic EQ 80Hz Band

D7	D6	D5	D4	D3	D2	D1	D0
			AGEQ4	AGEQ3	AGEQ2	AGEQ1	AGEQ0
			0	1	1	1	1

6.10.15Register – Graphic EQ 300Hz Band

D7	D6	D5	D4	D3	D2	D1	D0
			BGEQ4	BGEQ3	BGEQ2	BGEQ1	BGEQ0
			0	1	1	1	1

6.10.16Register – Graphic EQ 1kHz Band

D7	D6	D5	D4	D3	D2	D1	D0
			CGEQ4	CGEQ3	CGEQ2	CGEQ1	CGEQ0
			0	1	1	1	1

6.10.17Register – Graphic EQ 3kHz Band

D7	D6	D5	D4	D3	D2	D1	D0
			DGEQ4	DGEQ3	DGEQ2	DGEQ1	DGEQ0
			0	1	1	1	1

6.10.18Register – Graphic EQ 8kHz Band

D7	D6	D5	D4	D3	D2	D1	D0
			EGEQ4	EGEQ3	EGEQ2	EGEQ1	EGEQ0
			0	1	1	1	1

Table 28.

XGEQ(4..0)	Boost/Cut
11111	+16
11110	+15
11101	+14
…	…
10000	+1
01111	0
01110	-1
…	…
00001	-14
00000	-15

6.10.19Biquad Internal Channel Loop-Through

D7	D6	D5	D4	D3	D2	D1	D0
C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible inputs at the input to the biquad block as shown in figure X.

The input can be received from the output of that channels MIX#1 engine or from the output of bass/treble(Biquad#10) of the previous channel. In this scenario channel 1 would receive channel 8. This enables the use of more than 10 biquads on any given channel at the loss of the number of separate internal processing channels.

CxBLP:

0 - Input from Channel X MIX#1 engine output - normal operation

1 - Input from Channel X-1 biquad #10 output - loop operation

6.10.20Mix Internal Channel Loop-Through

D7	D6	D5	D4	D3	D2	D1	D0
C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible sets of inputs at the inputs to the Mix#1 block as shown in figure X. The inputs can be received from the outputs of the interpolation block as normally occurs(CxMXLP = 0) or the inputs can be received from the outputs of the Mix#2 block. This enables the ability to perform additional filtering after the second mix block at the expense of losing this processing capability on the channel.

CxMXLP:

0 - Inputs to Channel X MIX#1 engine from interpolation outputs - Normal Operation

1 - Inputs from Channel X MIX#1 engine from MIX#2 engine outputs - loop operation

6.10.21EQ Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQCBP	C3EQBP	C2EQBP	C1EQBP
0	0	0	0	0	0	0	0

EQ control can be bypassed on a per channel basis. If EQ control is bypassed on a given channel the prescale and all 10 filters (high-pass, biquads, de-emphasis, bass management cross-over, bass, treble in any combination) are bypassed for that channel.

CxEQBP:

0 – Perform EQ on Channel X – normal operation

1 – Bypass EQ on Channel X

6.10.22Tone Control Bypass

D7	D6	D5	D4	D3	D2	D1	D0
C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
0	0	0	0	0	0	0	0

Tone control(bass/treble) can be bypassed on a per channel basis. If tone control is bypassed on a given channel the two filters that tone control utilizes are made available as user programmable biquads #9 and #10.

6.10.23Tone Control

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

6.10.24 Tone Control Boost/Cut as a function of BTC and TTC bits.

BTC(3..0)/TTC(3..0)	Boost/Cut
0000	-12dB
0001	-12dB
…	…
0111	-4dB
0110	-2dB
0111	0dB
1000	+2dB
1001	+4dB
…	…
1101	+12dB
1110	+12dB
1111	+12dB

6.11 Dynamics Control

6.11.1 Channel Limiter Select Channels 1,2,3,4

D7	D6	D5	D4	D3	D2	D1	D0
C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0	0	0	0	0	0	0	0

6.11.2 Channel Limiter Select Channels 5,6,7,8

D7	D6	D5	D4	D3	D2	D1	D0
C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0	0	0	0	0	0	0	0

6.11.3 Limiter 1 Attack/Release Rate

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

6.11.4 Limiter 1 Attack/Release Threshold

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

6.11.5 Limiter 2 Attack/Release Rate

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

6.11.6 Limiter 2 Attack/Release Threshold

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

The STA308A includes 2 independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode or to actively reduce the dynamic range for a better listening environment such as a night-time listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in Configuration Register B, bit 7 address 0x02. Each channel can be mapped to either limiter or not mapped, meaning that channel will clip when 0dBFS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then if needed adjust the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers. It is recommended in anti-clipping mode to set this to 0dBFS, which corresponds to the maximum unclipped output power of a DDX amplifier. Since gain can be added digitally within the STA308A it is possible to exceed 0dBFS or any other LxAT setting, when this occurs, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through a RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the Release Rate register. The gain can never be increased past it's set value and therefore the release will only occur if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound "lifeless".

In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Figure 7. Basic Limiter and Volume Flow Diagram.

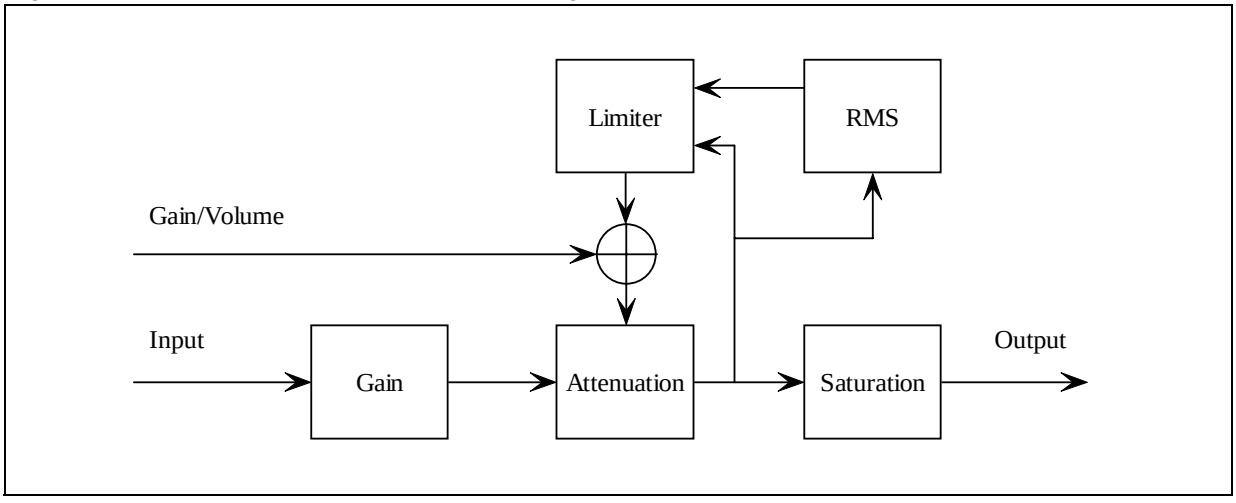


Table 29. Channel Limiter Mapping as a function of CxLS bits

CxLS(1,0)	Channel Limiter Mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

Table 30. Limiter Attack Rate as a function of LxA bits.

LxA(3..0)	Attack Rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	
1111	0.0451	Slow

Table 31. Limiter Release Rate as a function of LxR bits.

LxR(3..0)	Release Rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	
1111	0.0104	Slow

6.12 Anti-Clipping Mode

Table 32. Limiter Attack Threshold as a function of LxAT bits (AC-Mode).

LxAT(3..0)	AC(dB relative to FS)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 33. Limiter Release Threshold as a as a function of LxRT bits (AC-Mode).

LxRT(3..0)	AC(dB relative to FS)
0000	-∞
0001	-29dB
0010	-20dB
0011	-16dB
0100	-14dB
0101	-12dB
0110	-10dB
0111	-8dB
1000	-7dB
1001	-6dB
1010	-5dB
1011	-4dB
1100	-3dB
1101	-2dB
1110	-1dB
1111	-0dB

6.13 Dynamic Range Compression Mode

Table 34. Limiter Attack Threshold as a function of LxAT bits (DRC-Mode).

LxAT(3..0)	DRC(dB relative to Volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 35. Limiter Release Threshold as a as a function of LxRT bits (DRC-Mode).

LxRT(3..0)	DRC(db relative to Volume + LxAT)
0000	-∞
0001	-38dB
0010	-36dB
0011	-33dB
0100	-31dB
0101	-30dB
0110	-28dB
0111	-26dB
1000	-24dB
1001	-22dB
1010	-20dB
1011	-18dB
1100	-15dB
1101	-12dB
1110	-9dB
1111	-6dB

6.14 PWM Output Timing

6.14.1 Channel 1&2 Output Timing

D7	D6	D5	D4	D3	D2	D1	D0
	C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
	1	0	0		0	0	0

6.14.2 Channel 3&4 Output Timing

D7	D6	D5	D4	D3	D2	D1	D0
	C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
	1	1	0		0	1	0

6.14.3 Channel 5&6 Output Timing

D7	D6	D5	D4	D3	D2	D1	D0
	C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
	1	0	1		0	0	1

6.14.4 Channel 7&8 Output Timing

D7	D6	D5	D4	D3	D2	D1	D0
	C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
	1	1	1		0	1	1

The centering of the individual channel PWM output periods can be adjusted by the Output Timing registers. PWM slot settings can be chosen to insure that pulse transitions do not occur at the same time on different channels using the same power device. There are 8 possible settings, the appropriate setting varying based on the application and connections to the DDX power devices.

Table 36. Channel Output Timing as a function of CxOT bits.

CxOT(2..0)	PWM Slot
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

6.15 I2S Output Channel Mapping

6.15.1 Channel I2S Output Mapping Channels 1 & 2

D7	D6	D5	D4	D3	D2	D1	D0
	C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
	0	0	1		0	0	0

6.15.2 Channel I2S Output Mapping Channels 3 & 4

D7	D6	D5	D4	D3	D2	D1	D0
	C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
	0	1	1		0	1	0

6.15.3 Channel I2S Output Mapping Channels 5 & 6

D7	D6	D5	D4	D3	D2	D1	D0
	C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
	1	0	1		1	0	0

6.15.4 Channel I2S Output Mapping Channels 7 & 8

D7	D6	D5	D4	D3	D2	D1	D0
	C8OM2	C8M1	C8OM0		C7OM2	C7OM1	C7OM0
	1	1	1		1	1	0

Each I2S Output Channel can receive data from any channel output of the volume block. Which channel a particular I2S output receives is dependent upon that channels CxOM register bits.

Table 37. Channel Mapping as a function of CxOM bits.

CxOM(2..0)	Serial Output From
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

6.16 User-Defined Coefficient Control

6.16.1 Coefficient Address Register 1

D7	D6	D5	D4	D3	D2	D1	D0
						CFA9	CFA8
						0	0

6.16.2 Coefficient Address Register 2

D7	D6	D5	D4	D3	D2	D1	D0
CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0	0	0	0	0	0	0	0

6.16.3 Coefficient b1Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

6.16.4 Coefficient b1Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

6.16.5 Coefficient b1 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

6.16.6 Coefficient b2 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

6.16.7 Coefficient b2 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

6.16.8 Coefficient b2 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

6.16.9 Coefficient a1 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

6.16.10 Coefficient a1 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

6.16.11 Coefficient a1 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

6.16.12 Coefficient a2 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

6.16.13 Coefficient a2 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

6.16.14 Coefficient a2 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

6.16.15 Coefficient b0 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

6.16.16 Coefficient b0 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

6.16.17 Coefficient b0 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

6.16.18 Coefficient Write Control Register

D7	D6	D5	D4	D3	D2	D1	D0
						WA	W1
						0	0

Coefficients for EQ and Bass Management are handled internally in the STA308A via RAM. Access to this RAM is available to the user via an I2C register interface.

A collection of I2C registers are dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write of the coefficient(s) to RAM. The following are instructions for reading and writing coefficients.

6.17 Reading a coefficient from RAM

- write top 2-bits of address to I^2C register 3Bh
- write bottom 8-bits of address to I^2C register 3Ch
- read top 8-bits of coefficient in I^2C address 3Dh
- read middle 8-bits of coefficient in I^2C address 3Eh
- read bottom 8-bits of coefficient in I^2C address 3Fh

6.18 Reading a set of coefficients from RAM

- write top 2-bits of address to I^2C register 3Bh
- write bottom 8-bits of address to I^2C register 3Ch
- read top 8-bits of coefficient in I^2C address 3Dh
- read middle 8-bits of coefficient in I^2C address 3Eh
- read bottom 8-bits of coefficient in I^2C address 3Fh
- read top 8-bits of coefficient b2 in I^2C address 40h
- read middle 8-bits of coefficient b2 in I^2C address 41h
- read bottom 8-bits of coefficient b2 in I^2C address 42h
- read top 8-bits of coefficient a1 in I^2C address 43h
- read middle 8-bits of coefficient a1 in I^2C address 44h
- read bottom 8-bits of coefficient a1 in I^2C address 45h
- read top 8-bits of coefficient a2 in I^2C address 46h
- read middle 8-bits of coefficient a2 in I^2C address 47h

- read bottom 8-bits of coefficient a2 in I^2C address 48h
- read top 8-bits of coefficient b0 in I^2C address 49h
- read middle 8-bits of coefficient b0 in I^2C address 4Ah
- read bottom 8-bits of coefficient b0 in I^2C address 4Bh

6.19 Writing a single coefficient to RAM

- write top 2-bits of address to I^2C register 3Bh
- write bottom 8-bits of address to I^2C register 3Ch
- write top 8-bits of coefficient in I^2C address 3Dh
- write middle 8-bits of coefficient in I^2C address 3Eh
- write bottom 8-bits of coefficient in I^2C address 3Fh
- write 1 to W1 bit in I^2C address 4Ch

6.20 Writing a set of coefficients to RAM

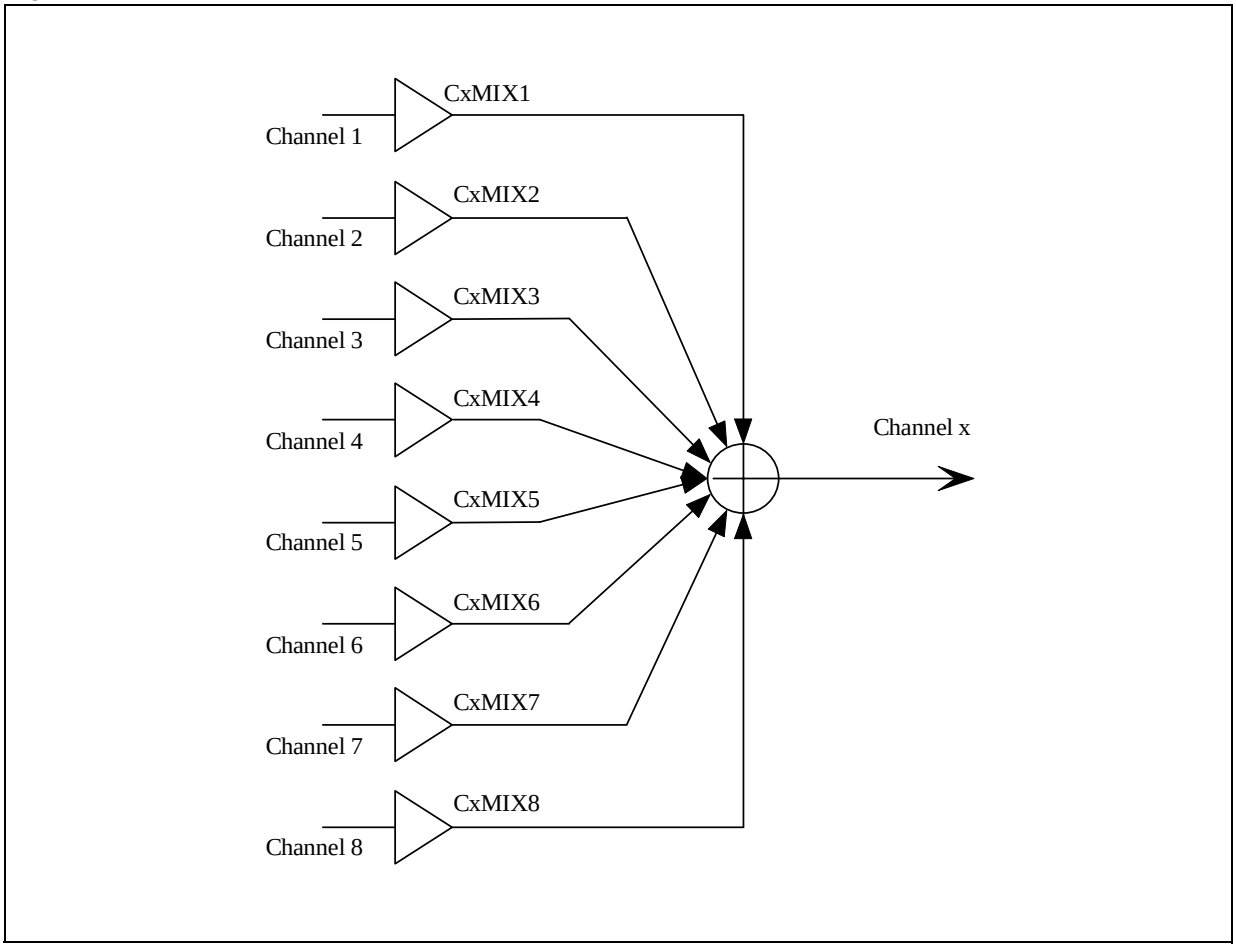
- write top 2-bits of starting address to I^2C register 3Bh
- write bottom 8-bits of starting address to I^2C register 3Ch
- write top 8-bits of coefficient b1 in I^2C address 3Dh
- write middle 8-bits of coefficient b1 in I^2C address 3Eh
- write bottom 8-bits of coefficient b1 in I^2C address 3Fh
- write top 8-bits of coefficient b2 in I^2C address 40h
- write middle 8-bits of coefficient b2 in I^2C address 41h
- write bottom 8-bits of coefficient b2 in I^2C address 42h
- write top 8-bits of coefficient a1 in I^2C address 43h
- write middle 8-bits of coefficient a1 in I^2C address 44h
- write bottom 8-bits of coefficient a1 in I^2C address 45h
- write top 8-bits of coefficient a2 in I^2C address 46h
- write middle 8-bits of coefficient a2 in I^2C address 47h
- write bottom 8-bits of coefficient a2 in I^2C address 48h
- write top 8-bits of coefficient b0 in I^2C address 49h
- write middle 8-bits of coefficient b0 in I^2C address 4Ah
- write bottom 8-bits of coefficient b0 in I^2C address 4Bh
- write 1 to WA bit in I^2C address 4Ch

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects.

When using this technique, the 10-bit address would specify the address of the biquad b1 coefficient (e.g. 0, 5, 10, 15, …, 100, … 395 decimal), and the STA308A will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

7 EQUALIZATION AND MIXING:

Figure 8.



7.1 Post-Scale

The STA308A provides one additional multiplication after the last interpolation stage and before the distortion compensation on each channel. This is a 24-bit signed fractional multiply.

The scale factor for this multiply is loaded into RAM using the same I2C registers as the biquad coefficients and the bass-management.

This post-scale factor can be used in conjunction with an ADC equipped micro-controller to perform power-supply error correction. All channels can use the channel 1 by setting the post-scale link bit.

Table 38. RAM Block for Biquads, Mixing, and Bass Management

Index (Decimal)	Index (Hex)		Coefficient	Default
0	00h	Channel 1 – Biquad 1	C1H10(b1/2)	000000h
1	01h		C1H11(b2)	000000h
2	02h		C1H12(a1/2)	000000h
3	03h		C1H13(a2)	000000h
4	04h		C1H14(b0/2)	400000h
5	05h	Channel 1 – Biquad 2	C1H20	000000h
…	…	…	…	…
49	31h	Channel 1 – Biquad 10	C1HA4	400000h
50	32h	Channel 2 – Biquad 1	C2H10	000000h
51	33h		C2H11	000000h
…	…	…	…	…
99	63h	Channel 2 – Biquad 10	C2HA4	400000h
100	64h	Channel 3 – Biquad 1	C3H10	000000h
…	…	…	…	…
399	18Fh	Channel 8 – Biquad 10	C8HA4	400000h
400	190h	Channel 1 – Pre-Scale	C1PreS	7FFFFFh
401	191h	Channel 2 – Pre-Scale	C2PreS	7FFFFFh
402	192h	Channel 3 – Pre-Scale	C3PreS	7FFFFFh
…	…	…	…	…
407	197h	Channel 8 – Pre-Scale	C8PreS	7FFFFFh
408	198h	Channel 1 – Post-Scale	C1PstS	7FFFFFh
409	199h	Channel 2 – Post-Scale	C2PstS	7FFFFFh
…	…	…	…	…
415	19Fh	Channel 8 – Post-Scale	C8PstS	7FFFFFh
416	1A0h	Channel 1 – Mix#1 1	C1MX11	7FFFFFh
417	1A1h	Channel 1 – Mix#1 2	C1MX12	000000h
…	…	…	…	…
423	1A7h	Channel 1 – Mix#1 8	C1MX18	000000h
424	1A8h	Channel 2 – Mix#1 1	C2MX11	000000h
425	1A9h	Channel 2 – Mix#1 2	C2MX12	7FFFFFh
…	…	…	…	…
463	1CFh	Channel 8 – Mix#1 8	C8MX18	7FFFFFh
464	1D0h	Channel 1 – Mix#2 1	C1MX21	7FFFFFh
465	1D1h	Channel 1 – Mix#2 2	C1MX22	000000h
…	…	…	…	…
471	1D7h	Channel 1 – Mix#2 8	C1MX28	000000h
472	1D8h	Channel 2 – Mix#2 1	C2MX21	000000h
473	1D9h	Channel 2 – Mix#2 2	C2MX22	7FFFFFh
…	…	…	…	…
527	20Fh	Channel 8 – Mix#2 8	C8MX28	7FFFFFh

7.2 Variable Max Power Correction:

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1

7.2.1 .

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	1	0	1	1	0	1

7.2.2

D7	D6	D5	D4	D3	D2	D1	D0
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

7.3 Variable Distortion Compensation:

DCC bits determine the 16 MSBs of the Distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1

7.3.1 .

D7	D6	D5	D4	D3	D2	D1	D0
DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
1	1	1	1	0	0	1	1

7.3.2

D7	D6	D5	D4	D3	D2	D1	D0
DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0	0	1	1	0	0	1	1

7.4 PSCorrect:

ADC is used to input ripple data to SDI78. The left channel(7) is used internally. No audio data can therefore be used on these channels. Though all channel mapping and mixing from other inputs to channels 7 and 8 internally are still valid.

7.4.1 Ripple Correction Value - RCV

Equivalent to negative maximum ripple peak as a percentage of Vcc (MPR), scaled by the inverse of maximum ripple p-p as percentage of full-scale analog input to ADC. Represented as a 1.11 signed fractional number.

7.4.2 Correction Normalization Value - CNV

Equivalent to 1/(1+MPR) expressed as a 0.12 unsigned fractional number.

7.4.3

D7	D6	D5	D4	D3	D2	D1	D0
RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0	0	0	0	0	0	0	0

7.4.4

D7	D6	D5	D4	D3	D2	D1	D0
RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0	0	0	0	1	1	1	1

7.4.5

D7	D6	D5	D4	D3	D2	D1	D0
CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0
1	1	1	1	1	1	1	1

7.5 QSurround5.1 Control Register:

D7	D6	D5	D4	D3	D2	D1	D0
					Qsfs	Qfour	Qen
					0	0	0

7.5.1 Qen: 1-QSurround5.1 automode enabled, if security enabled

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	Qen	0 – QSurround5.1 Automode Disabled 1 – QSurround5.1 Automode Enabled

7.5.2 Qfour: 0-5.1 mode, 1-4.1 mode

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	Qfour	0 – 5.1 QSurround Output Mode 1 – 4.1 QSurround Output Mode(No Center)

7.5.3 Qsfs : 0 – 48kHz input sample rate, 1 – 44.1

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	Qsfs	0 – 48/96/192kHz Input Sample Frequency 1 – 44.1/88.2/176.4kHz Input Sample Frequency

QSurround requires the use of both Mix#1 and Mix#2 blocks for channels 1-6, it also utilizes Biquad #8 on all channels. Inputs must be mapped to Channel 1/Left and Channel 2/Right.

Channel outputs are in standard DDX8001 configuration. XO crossover bits will determine internal crossover point. Enabling AMBMXE bit will place crossover filters on all channels. Either a 4.1 or 5.1 output mode can be selected via the Qfour bit. All AutoModes excluding De-emphasis are still available when QSurround is enabled.

7.5.4 Qsound security Enable:

A 16-bit register is provided, an exact number that is contained in the "Qsec Enable List"(separate document) must be put into this register for the Qsurround5.1 automode to be enabled.

7.5.5

D7	D6	D5	D4	D3	D2	D1	D0
QSEC15	QSEC14	QSEC13	QSEC12	QSEC11	QSEC10	QSEC9	QSEC8

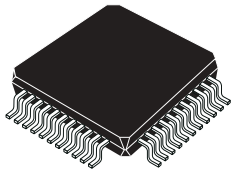
7.5.6

D7	D6	D5	D4	D3	D2	D1	D0
QSEC7	QSEC6	QSEC5	QSEC4	QSEC3	QSEC2	QSEC1	QSEC0

Figure 9. TQFP44 (10 x 10 x 1.4mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0˚(min.), 3.5˚(typ.), 7˚(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)

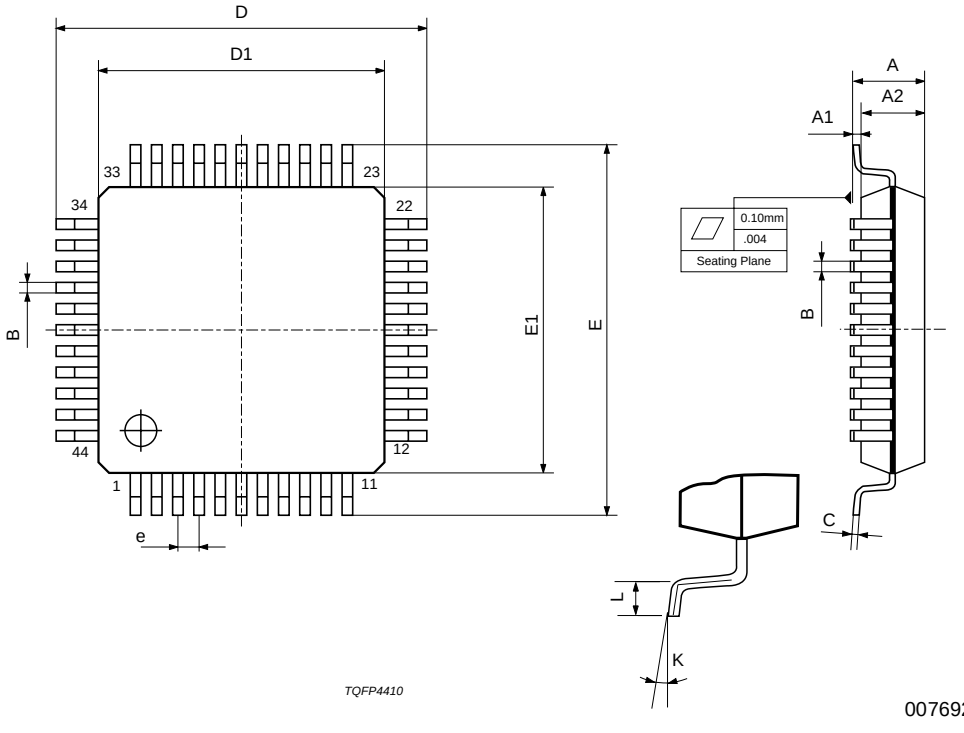


Table 39. Revision History

Date	Revision	Description of Changes
May 2004	1	First Issue

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